AMENDMENTS TO THE CLAIMS

1. (currently amended) A method for protecting a first boot area of a plurality of boot areas of a synchronous memory device, the method comprising:

transferring a protect status bit from a non-volatile register to a corresponding volatile register at power-up of the memory device;

initiating an erase operation to the first boot area;

reading ~~data~~ the protect status bit from ~~a~~ the volatile register ~~circuit~~ and detecting a security voltage; and

authorizing the erase operation to the first boot area if the protect status bit ~~data~~ is in a first state or the security voltage exceeds a predetermined voltage.

2. (currently amended) The method of claim 1 further comprising:
checking a status of a detection circuit if the protect status bit ~~data~~ is in a second state; and
authorizing the write operation to the first boot area based on an output of the detection circuit.

3. (original) The method of claim 2 wherein the detection circuit monitors an externally provided signal applied to the memory device.

4. (previously presented) The method of claim 1 wherein the plurality of boot areas comprise memory cells located at least significant and most significant addressable memory sectors of the synchronous memory device.

5. (currently amended) A memory device comprising:

an array of memory cells comprising a first and a second boot area that are located at least significant and most significant memory sectors of the array;

a non-volatile register that stores protect status bits corresponding to a protect status of each boot area;

a volatile data register ~~that stores~~ into which the protect status bits are transferred when the memory device is powered-up ~~corresponding to a protect status of each boot area~~; and

a state machine ~~capable of executing~~ adapted to transfer the protect status bits and execute a method of erasing each boot area including initiating an erase operation to either the first or the second boot area, reading the protect status bits from the volatile data register,

determining a voltage level of a security voltage, and authorizing the erase operation to one of the first or the second boot area if the protect status bits are in a first state or the security voltage is greater than a predetermined voltage.

6. (currently amended) A memory device comprising:

an array of memory cells having a first and a second boot area;

a non-volatile data register that stores protect status bits indicating a protect status of the at least one boot area;

a volatile data register corresponding to the non-volatile data register such that the protect status bits are transferred from the non-volatile data register to the volatile data-register;

a security voltage input that provides a security function for the first and second boot areas; and

control circuitry coupled to the non-volatile and volatile registers and the security voltage input to selectively prevent erase operations from being performed on the at least one boot area in response to a state of the protect status bits and the voltage level of the security voltage, the control circuitry adapted to transfer the protect status bits from the non-volatile data register to its corresponding volatile data register at power-up of the memory device.

7. (canceled)

8. (currently amended) A method for erasing a boot area of a plurality of boot areas of a flash memory device, the method comprising:

transferring a protect status bit from a non-volatile data register to a corresponding volatile data register upon power-up of the memory device;

initiating an erase operation to the boot area;

reading the protect status bit from the volatile data register; ~~and~~

reading a security voltage; and

authorizing the erase operation to the boot area if the protect status bit is in a first state or the security voltage is greater than a predetermined voltage.

9. (canceled)

10. (previously presented) The method of claim 8 and further including writing data to a second boot area of the plurality of boot areas when the first boot area no longer has sufficient capacity to hold additional data.